EXHIBIT 024

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
"Integrated circuit with data communication network and IC design method"

'2893 Patent Claim	Samsung Exynos 1280 System on Chip[1]
10. A method of designing an integrated circuit comprising a plurality of functional blocks, and a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks	Without conceding that the preamble of claim 10 of the '2893 Patent is limiting, Samsung Electronics Co., Ltd. (hereinafter, "Samsung") performs a method of designing an integrated circuit comprising a plurality of functional blocks, and a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks, either literally or under the doctrine of equivalents. For example, Samsung designs integrated circuits, including the Exynos 1280 system on chip (together, the "Exynos SoC").

[1] The Exynos system on chip is charted as a representative product made used, sold, offered for sale, and/or imported by Samsung. The citations to evidence contained herein are illustrative and should not be understood to be limiting. The right is expressly reserved to rely upon additional or different evidence, or to rely on additional citations to the evidence cited already cited herein.

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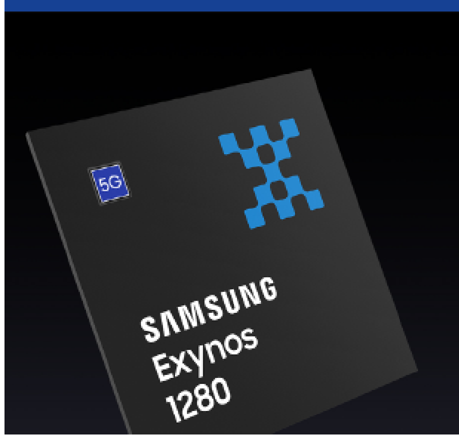
SAMSUNG

Product brief
Create infinite possibilities

Exynos 1280

Highlights

A mobile processor ready for 5G and AI
Advanced ISP and MFC for rich multimedia experience
Powerful octa-core CPU and GPU



5G for all

Exynos 1280 is a mobile processor based on a 64-bit RISC processor. It contains a 5G modem, which is compliant with two types of 5G network (Sub-6GHz and mmWave), as well as all legacy networks. It is built using an advanced 5nm EUV process for high power efficiency.

All-in-one processor for 5G

The Exynos 1280 embedded modem supports both sub-6GHz (Frequency Range

https://semiconductor.samsung.com/resources/brochure/Exynos1280.pdf

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The Exynos SoC includes a plurality of functional blocks, for example Arm Cortex-A78 core, Cortex-A55 core, Arm Mali-G68 GPU, and AI Engine with NPU:

Specifications

	Exynos 1280
CPU	Cortex®-A78 x 2 + Cortex®-A55 x 6
GPU	Mali™-G68
AI	AI Engine with NPU
Modem	5G NR Sub-6GHz 2.55Gbps (DL) / 1.28Gbps (UL) 5G NR mmWave 1.84Gbps (DL) / 0.92Gbps (UL) LTE Cat.18 6CC 1.2Gbps (DL) / Cat.18 2CC 200Mbps (UL)
Connectivity	WiFi 802.11ac MIMO with Dual-band (2.4/5G), Bluetooth® 5.2, FM Radio Rx
GNSS	Quad-constellation multi-signal for L1 and L5 GNSS
Camera	Up to 108MP in single camera mode, Single-camera 32MP @30fps
Video	4K 30fps encoding and decoding
Display	Full HD+@120Hz
Memory	LPDDR4x
Storage	UFS v2.2
Process	5nm

https://semiconductor.samsung.com/resources/brochure/Exynos1280.pdf

The Exynos SoC utilizes Arteris network on chip interconnect technology, and/or a derivative thereof, (collectively, the "Arteris NoC") as a data communication network:

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	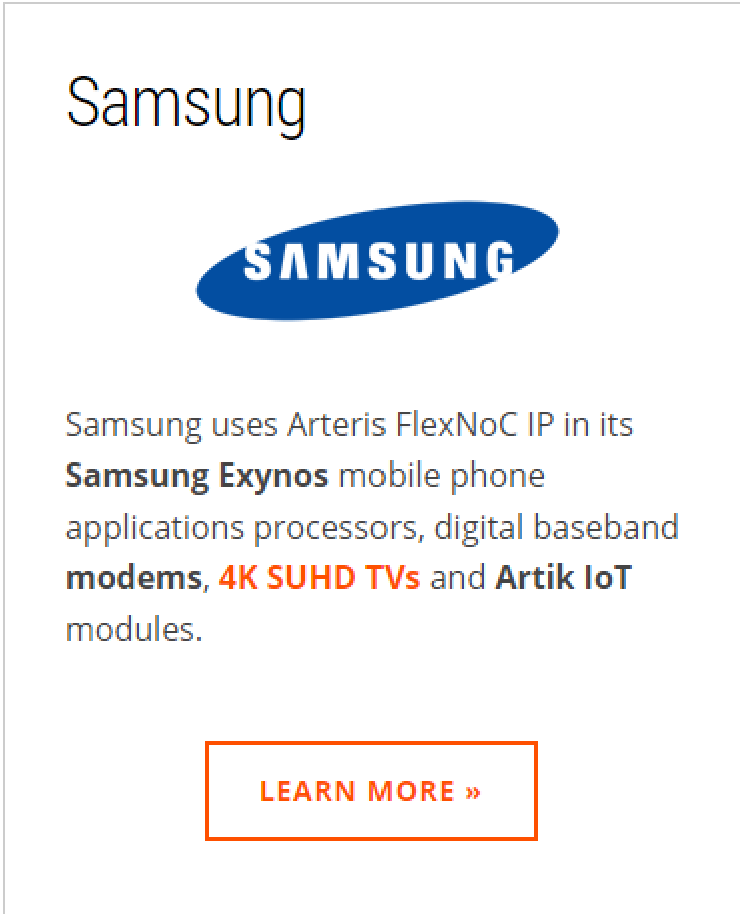 https://web.archive.org/web/20210514110614/https://www.arteris.com/customers

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'2893 Patent Claim	Samsung Exynos 1280 System on Chip[1]
	Arteris IP FlexNoC® Interconnect Licensed by Samsung's System LSI Business for Digital TV Chips by **Kurt Shuler**, on April 23, 2019 CAMPBELL, Calif. –April 23, 2019– Arteris IP, the world's leading supplier of innovative, silicon-proven network-on-chip (NoC) interconnect semiconductor intellectual property, today announced that Samsung's System LSI Business has renewed multiple Arteris IP FlexNoC Interconnect licenses for use in multiple high-performance digital TV (DTV) processing chips utilizing Samsung's latest semiconductor technology process nodes. *"Over many years, FlexNoC interconnect IP has helped us accelerate implementation of our digital TV chip designs on our latest semiconductor process nodes. This core interconnect technology is required to develop complex and highly optimized chips in a predictable, low-risk fashion."* SAMSUNG *Jaeyoul Lee, Vice President, **Samsung Electronics*** Samsung first licensed FlexNoC interconnect IP in 2010. Since then, Samsung has used Arteris interconnect IP to enable complex SoC architectures in chips like the Exynos mobile processors and other electronic systems. https://www.arteris.com/press-releases/samsung-lsi-dtv-arteris-ip-flexnoc

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	Arteris Interconnect IP Solution Selected by Samsung for Mobile SoC Deployment by **Kurt Shuler**, on November 02, 2010 Network-on-Chip (NoC) interconnect technology leader enables higher performance and more cost effective designs for mobile phone systems-on-chip (SoCs) SUNNYVALE, California — November 2, 2010 — Arteris, Inc., a leading supplier of on-chip interconnect IP solutions, today announced that Samsung Electronics Co., Ltd., has selected Arteris' interconnect solutions for multiple chips within Samsung's mobile SOC products. Samsung chose Arteris interconnect IP to support the high speed inter-chip communication requirements in next generation mobile SOC products. *"The Arteris interconnect IP offers us a convenient solution to handle the high speed communication needed between our SoC and external modem IC. Our customers will benefit from the lower BOM cost and power consumption as a result of this IP. We look forward to Arteris' interconnect IP helping us shorten development schedules and lower risks associated with compatibility.* SAMSUNG *Thomas Kim, Vice President, SoC Platform Development, System LSI,* ***Samsung Electronics*** https://www.arteris.com/press-releases/pr_2010_nov_02?hsLang=en-us

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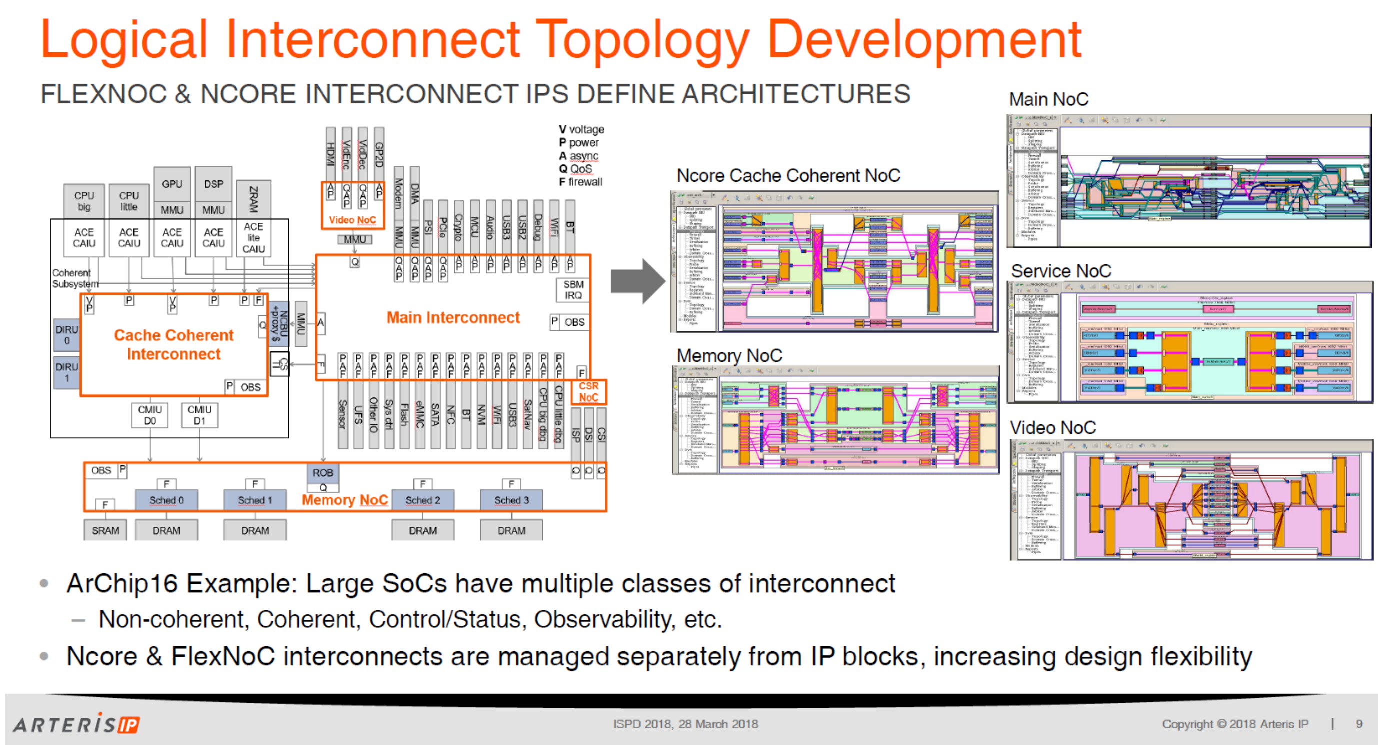
	A large SoC, such as the Exynos SoC may include multiple classes of Arteris NoC data communication network:



See Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 9.

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'2893 Patent Claim	Samsung Exynos 1280 System on Chip[1]
	The Arteris NoC in the Exynos SoC is a data communication network comprising a plurality of network stations being interconnected via a plurality of communication channels for communicating data packages between the functional blocks. For example, the Arteris NoC uses Network Interface Units (NIUs) "at the boundary of the NoC" and which "connect[] IP blocks to the network": ***11.3.1.1 Transaction Layer*** The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets

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'2893 Patent Claim	Samsung Exynos 1280 System on Chip[1]
	on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313; *see id* at 308 (explaining that Chapter 11 of this book describes the function of the Arteris NoC: "In this chapter we will present an MPSoC platform […] using Arteris NoC as communication infrastructure."). As a further illustration, in the Arteris NoC, "[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network…. Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path."

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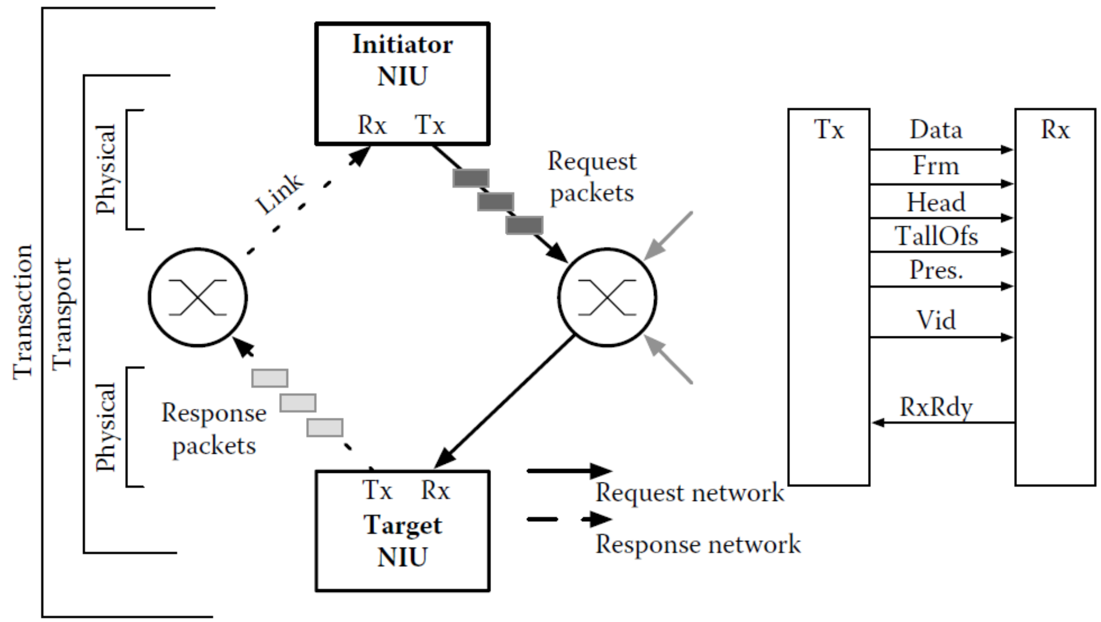
'2893 Patent Claim	Samsung Exynos 1280 System on Chip[1]
	 **FIGURE 11.1** NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312.
each data package comprising N data elements including a data	Without conceding that the preamble of claim 10 of the '2893 Patent is limiting, in the Arteris NoC utilized by the Exynos SoC, each data package comprising N data elements including a data element comprising routing information for the network stations, N being an integer of at least two, either literally or under the doctrine of equivalents.

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'2893 Patent Claim	Samsung Exynos 1280 System on Chip[1]
element comprising routing information for the network stations, N being an integer of at least two	For example, the "Arteris NTTP protocol is packet-based" and the packets, which have "header and necker cells [that] contain information relative to routing, payload size, packet type, and the packet target address," are "transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes": ***11.3.1.2 Transport Layer*** The Arteris NTTP protocol is packet-based. Packets created by NIUs are transported to other parts of the NoC to accomplish the transactions that are required by foreign IP nodes. All packets are comprised of cells: a header cell, an optional necker cell, and possibly one or more data cells (for packet definition see Figure 11.2; further descriptions of the packet can be found in the next subsection). The header and necker cells contain information relative to routing, payload size, packet type, and the packet target address. Formats for request packets and response packets are slightly different, with the key difference being the presence of an additional cell, the necker, in the request packet to provide detailed addressing information to the target. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313. As yet a further illustration, packets in the Arteris NoC are "delivered as words that are sent along links and "[o]ne link (represented in Figure 11.1) defines the following signals":

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	maximum cell-width (header, necker, and data cell) and the link-width. One link (represented in Figure 11.1) defines the following signals: • **Data**—Data word of the width specified at design-time. • **Frm**—When asserted high, indicates that a packet is being transmitted. • **Head**—When asserted high, indicates the current word contains a packet header. When the link-width is smaller than single (SGL), the header transmission is split into several word transfers. However, the Head signal is asserted during the first transfer only. • **TailOfs**—Packet tail: when asserted high, indicates that the current word contains the last packet cell. When the link-width is smaller than single (SGL), the last cell transmission is split into several word transfers. However, the Tail signal is asserted during the first transfer only. • **Pres.**—Indicates the current priority of the packet used to define preferred traffic class (or Quality of Service). The width is fixed during the design time, allowing multiple pressure levels within the same NoC instance (bits 3–5 in Figure 11.2). • **Vld**—Data valid: when asserted high, indicates that a word is being transmitted. • **RxRdy**—Flow control: when asserted high, the receiver is ready to accept word. When de-asserted, the receiver is busy. This signal set, which constitutes the Media Independent NoC Interface (MINI), is the foundation for NTTP communications.

'2893 Patent Claim	Samsung Exynos 1280 System on Chip[1]
	Id. at 313-314. As a further example, the packets sent in the Arteris NoC are "composed of cells that are organized into fields, with each field carrying specific information":

Field	Size	Function
Opcode	4 bits/3 bits	Packet type: 4 bits for requests, 3 bits for responses
MstAddr	User Defined	Master address
SlvAddr	User Defined	Slave address
SlvOfs	User Defined	Slave offset
Len	User Defined	Payload length
Tag	User Defined	Tag
Prs	User defined (0 to 2)	Pressure
BE	0 or 4 bits	Byte enables
CE	1 bit	Cell error
Data	32 bits	Packet payload
Info	User Defined	Information about services supported by the NoC
Err	1 bit	Error bit

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StartOfs	2 bits	Start offset
StopOfs	2 bits	Stop offset
WrpSize	4 bits	Wrap size
Rsv	Variable	Reserved
CtlId	4 bits/3 bits	Control identifier, for control packets only
CtlInfo	Variable	Control information, for control packets only
EvtId	User defined	Event identifier, for event packets only

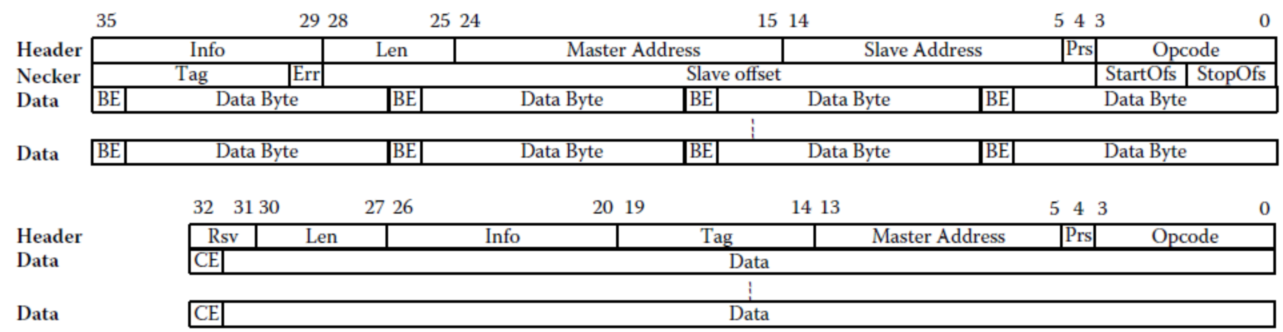

FIGURE 11.2
NTTP packet structure.

Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 313, 314-315.

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the plurality of network stations comprising a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface	Without conceding that the preamble of claim 10 of the '2893 Patent is limiting, in the Arteris NoC utilized by the Exynos SoC, the plurality of network stations comprise a plurality of data routers and a plurality of network interfaces, each of the data routers being coupled to a functional block via a network interface, either literally or under the doctrine of equivalents. For example, the Arteris NoC uses Network Interface Units (NIUs) "at the boundary of the NoC" and which "connect[] IP blocks to the network": ***11.3.1.1 Transaction Layer*** The transaction layer is compatible with bus-based transaction protocols used for on-chip communications. It is implemented in NIUs, which are at the boundary of the NoC, and translates between third-party and NTTP protocols. Most transactions require the following two-step transfers: • A master sends request packets. • Then, the slave returns response packets. As shown in Figure 11.1, requests from an initiator are sent through the master NIU's transmit port, Tx, to the NoC request network, where they are routed to the corresponding slave NIU. Slave NIUs, upon reception of request packets

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	on their receive ports, Rx, translate requests so that they comply with the protocol used by the target third-party IP node. When the target node responds, returning responses are again converted by the slave NIU into appropriate response packets, then delivered through the slave NIU's Tx port to the response network. The network then routes the response packets to the requesting master NIU, which forwards them to the initiator. At the transaction level, NIUs enable multiple protocols to coexist within the same NoC. From the point of view of the NTTP modules, different third-party protocols are just packets moving back and forth across the network. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 311, 312-313. As a further illustration, in the Arteris NoC, "[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response packets that are exchanged between a slave NIU and a master NIU through the response network…. Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path."

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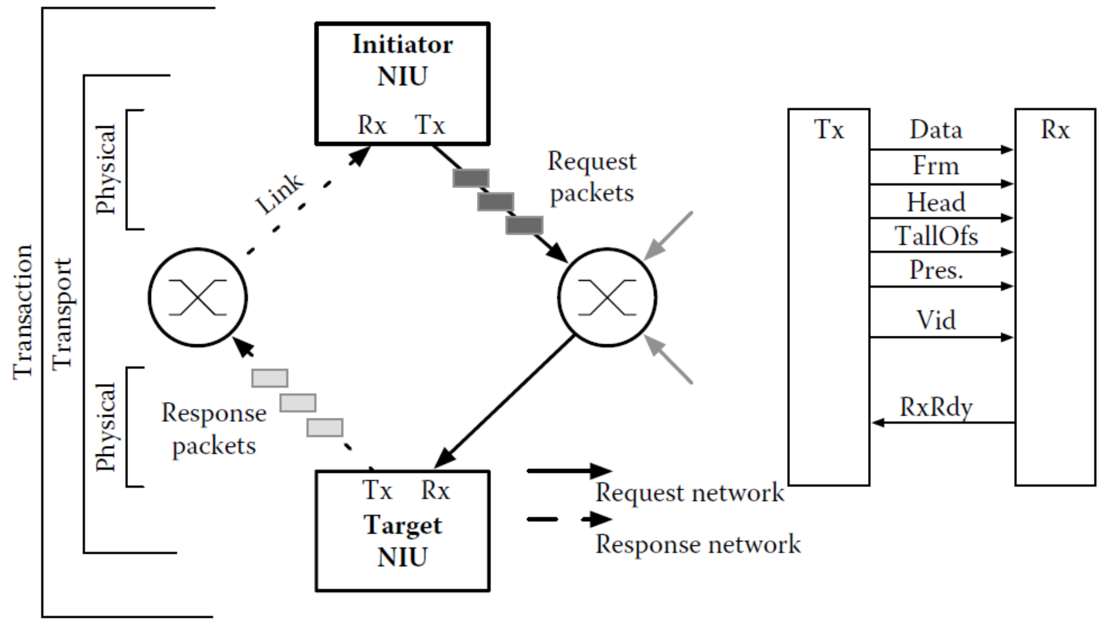
'2893 Patent Claim	Samsung Exynos 1280 System on Chip[1]
	 **FIGURE 11.1** NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312. As a further illustration of the routers in the Arteris NoC:

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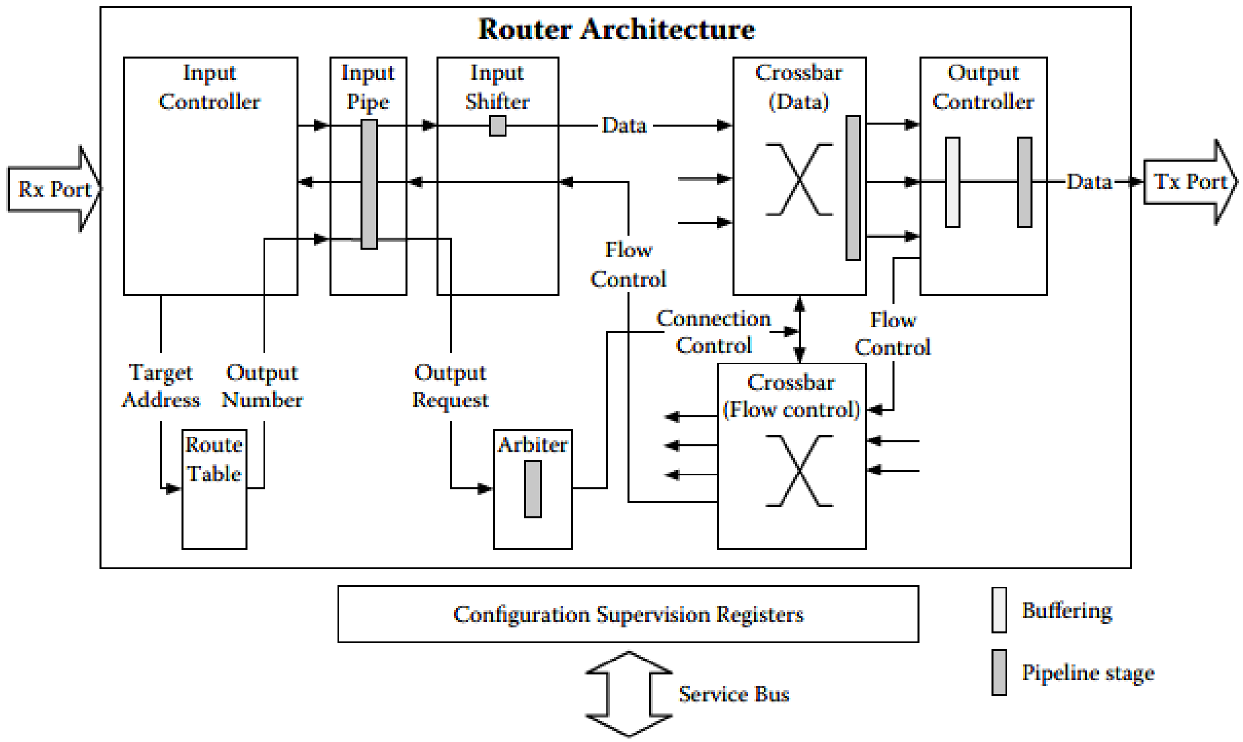
	11.3.3.2 Routing The switch extracts the destination address and possibly the scattering information from the incoming packet header and necker cells, and then selects an output port accordingly. For a request switch, the destination address is the slave address and the scattering information is the master address  **FIGURE 11.6** Packet transportation unit: Router architecture.

'2893 Patent Claim	Samsung Exynos 1280 System on Chip[1]
	As a further illustration of the network interfaces in the Arteris NoC: ***11.3.2.1 Initiator NIU Units*** Initiator NIU units (the architecture of the AHB initiator is given in Figure 11.4) enable connection between an AMBA-AHB master IP and the NoC. It translates AHB transactions into an equivalent NTTP packet sequence, and transports requests and responses to and from a target NIU, that is, slave IP (slave can be any of the supported protocols). The AHB-to-NTTP unit instantiates a Translation Table for address decoding. This table receives 32-bit AHB addresses from the NIU and returns the packet header and necker information that is needed to access the NTTP address space: Slave address, Slave offset, Start offset, and the coherency size (see Figure 11.2). Whenever the AHB address does not fit the predefined decoding range, the table asserts an error signal that sets the error bit of the corresponding NTTP request packet, for further error handling by the NoC. The translation table is fully user-defined at design time: it must first be completed with its own hardware parameters, then passed to the NIU. Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 317.

'2893 Patent Claim	Samsung Exynos 1280 System on Chip[1]
	11.3.2.2 Target NIU Units Target NIU units enable connection of a slave IP to the NoC by translating NTTP packet sequences into equivalent packet transactions, and transporting requests and responses to and from targets (the architecture of the AHB Target NIU is given in Figure 11.5). For the AHB target NIU, the AHB address space is mapped from the NTTP address space using the slave offset, the start/stop offset, and the slave address fields, when applicable (from the header of the request packet, Figure 11.2). The AHB address bus is always *Id.* at 318.
the method comprising the acts of: identifying a first communication channel between a first network station and a second network station that has a data transfer delay exceeding a	The method of designing the Exynos SoC includes identifying a first communication channel between a first network station and a second network station that has a data transfer delay exceeding a predefined delay threshold, either literally or under the doctrine of equivalents. For example, when a signal cannot cross a chip in one clock cycle, designing the Exynos SoC including the Arteris NoC includes pipelining for distance spanning. As an illustration, a signal traveling "~6mm" has a propagation delay of "~400ps/mm", requiring at least "2400ps to span the Distance"; thus requiring "at least 3 pipeline stages and 4 clock cycles to meet timing."

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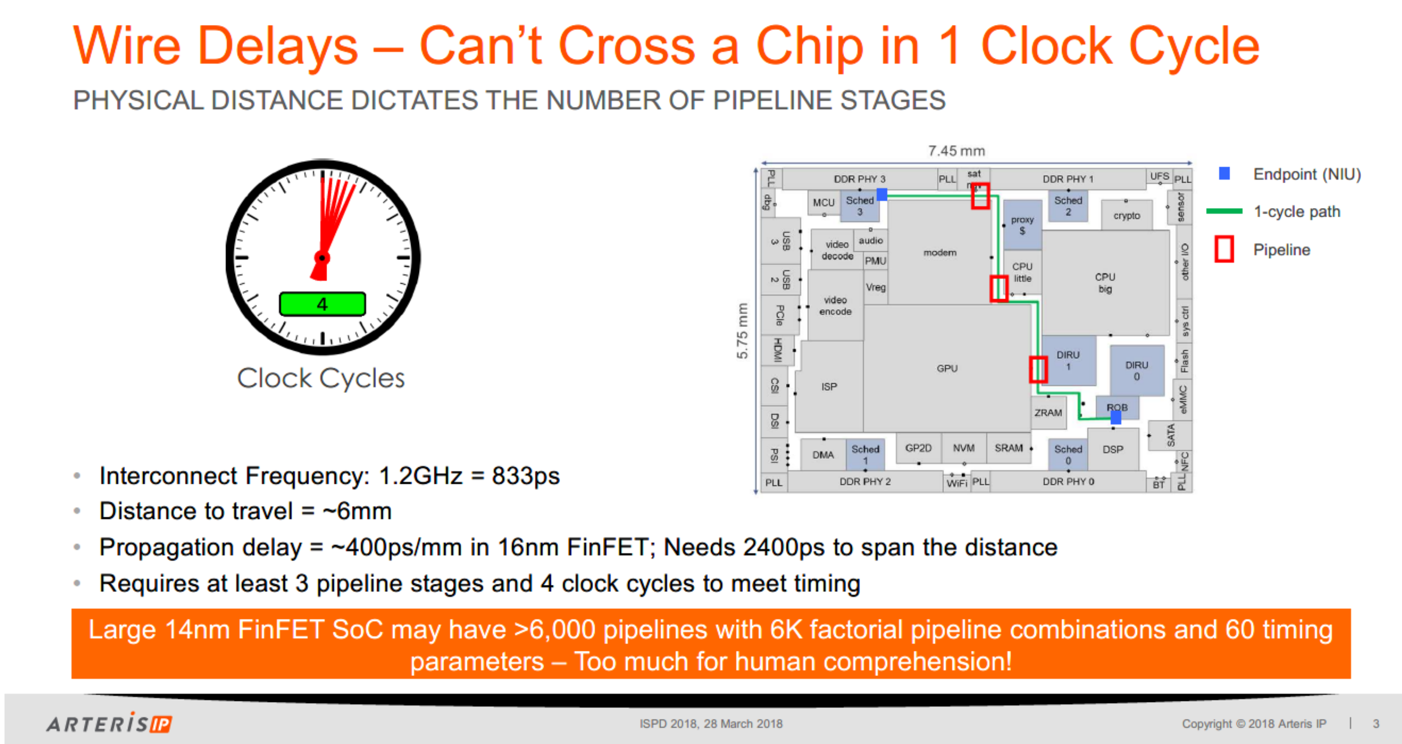
predefined delay threshold; and	 *See* Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 3.
in response to the identifying act, inserting M*N data storage elements into the data	In response to the identifying act, method of designing the Exynos SoC includes inserting M*N data storage elements into the data communication network, M being a positive integer, for introducing a delay of M*N cycles on the first communication channel, either literally or under the doctrine of equivalents. For example, in the Arteris NoC, "[a]n NTTP transaction is typically made of request packets, traveling through the request network between the master and the slave NIUs, and response

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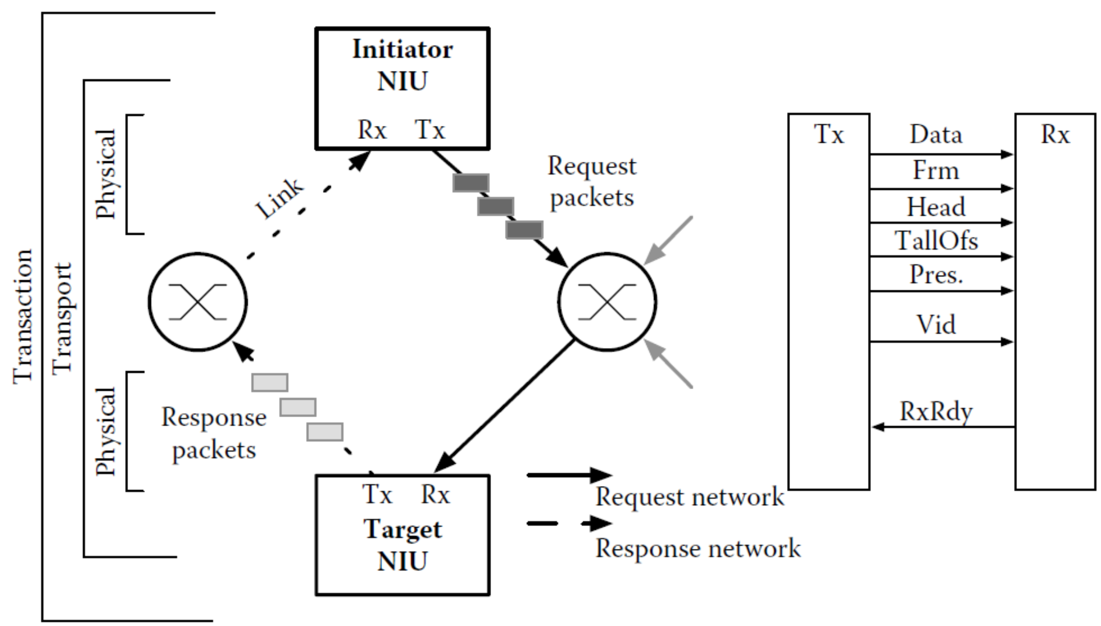
communication network, M being a positive integer, for introducing a delay of M*N cycles on the first communication channel.	packets that are exchanged between a slave NIU and a master NIU through the response network.… Transactions are handed off to the transport layer, which is responsible for delivering packets between endpoints of the NoC (using links, routers, muxes, rated adapters, FIFOs, etc.). Between NoC components, packets are physically transported as cells across various interfaces, a cell being a basic data unit being transported. This is illustrated in Figure 11.1, with one master and one slave node, and one router in the request and response path."  **FIGURE 11.1** NTTP protocol layers mapped on NoC units and Media Independent NoC Interface—MINI.

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	See Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 312. As a further example, a "delay pipeline is automatically inserted in the input controller to keep data and routing information in phase" and an input pipe "introduces a one-word-deep FIFO": Depending on the kind of routing table chosen, more than one cycle may be required to make a decision. A delay pipeline is automatically inserted in the input controller to keep data and routing information in phase, thus guaranteeing one-word-per-cycle peak throughput. Routing tables select the output port that a given packet must take. The route decision is based on the * * * The input pipe is optional and may be inserted individually for each input port. It introduces a one-word-deep FIFO between the input controller and the crossbar and can help timing closure, although at the expense of one supplementary latency cycle. *See* Networks-On-Chips Theory and Practice, https://vdoc.pub/download/networks-on-chips-theory-and-practice-embedded-multi-core-systems-6f26qivv11f0, at 322. As a further example the crossbar may have pipeline storage elements and the output controller contains a FIFO storage element "with as many words as there are date pipelined in the crossbar":

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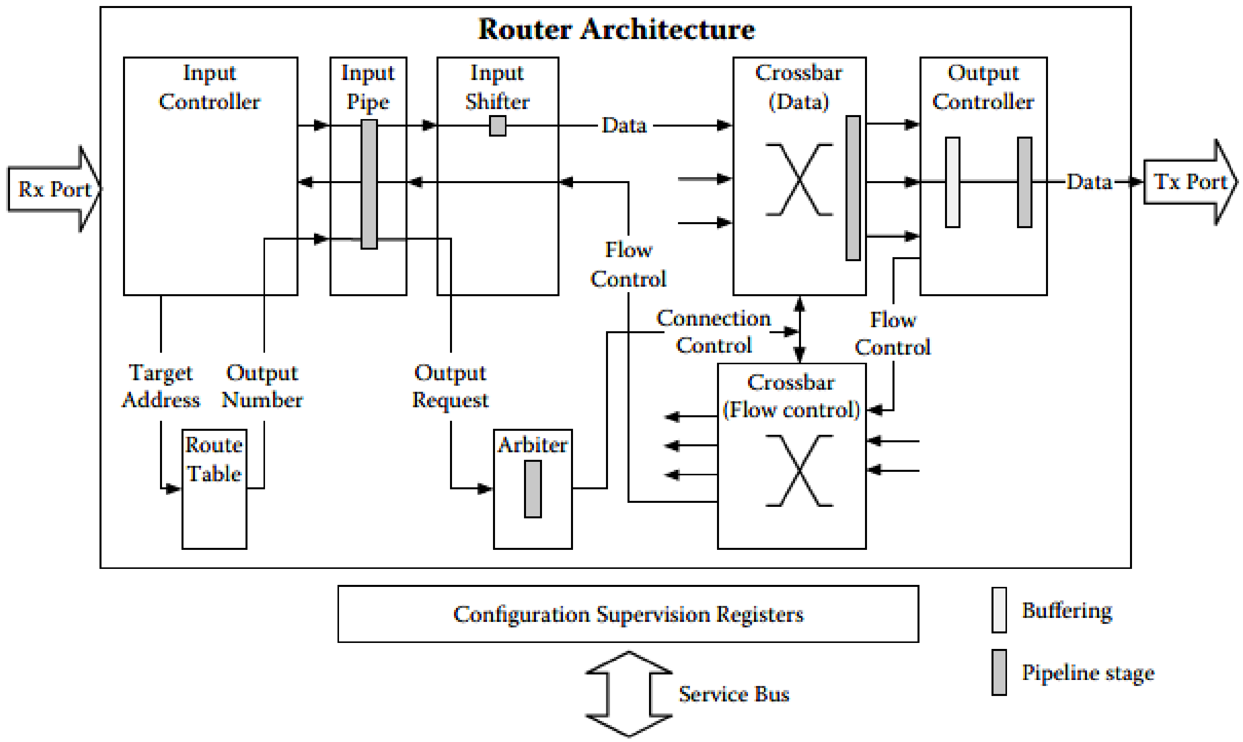
	The crossbar implements datapath connection between inputs and outputs. It uses the connection matrix produced by the arbiter to determine which connections must be established. It is equivalent to a set of m muxes (one per output port), each having n inputs (one per input port). If necessary, the crossbar can be pipelined to enhance timing. The number of pipeline stages can be as high as $max(n, m)$. The output controller constructs the output stream. It is also responsible for compensating crossbar latency. It contains a FIFO with as many words as there are data pipelined in the crossbar. FIFO flow control is internally managed with a credit mechanism. Although FIFO is typically empty, should the output port become blocked, it contains enough buffering to flush the crossbar. When necessary for timing reasons, a pipeline stage can be introduced at the output of the controller. *Id.* at 323. The buffering and pipeline stages are shown in the following depiction of the router architecture of the Arteris NoC:

	11.3.3.2 Routing The switch extracts the destination address and possibly the scattering information from the incoming packet header and necker cells, and then selects an output port accordingly. For a request switch, the destination address is the slave address and the scattering information is the master address  **FIGURE 11.6** Packet transportation unit: Router architecture.

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	Id. at 320. As another example, the "fwdPipe" parameter "introduces a true pipeline register on the forward signals" and "inserts the DFFs required to register a full data word as well as with control signals, and a cycle delay is inserted for packets traveling this path": get frequency, process, or floor plan. The opportunity to break long paths is present on most MINI transmission ports, and is controlled through a parameter named fwdPipe: when set, this parameter introduces a true pipeline register on the forward signals, and effectively breaks the forward path. The parameter inserts the DFFs required to register a full data word as well as with control signals, and a cycle delay is inserted for packets traveling this path. *Id.* at 323-324. As another example, pipelines may be automatically inserted by the Arteris NoC to close timing:

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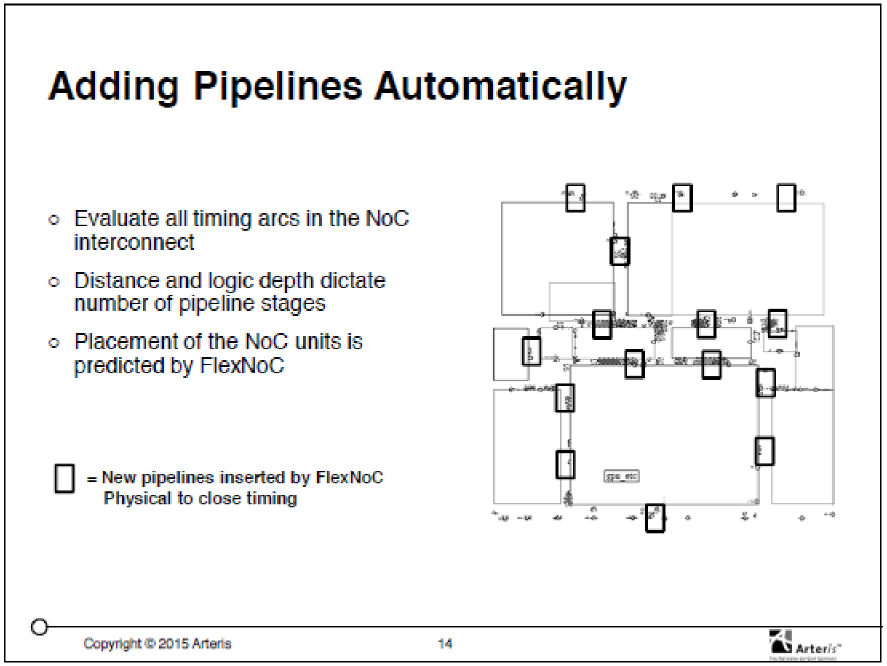
'2893 Patent Claim	Samsung Exynos 1280 System on Chip[1]
	 Using SoC Interconnect IPs to Improve Physical Layout, http://mpsoc-forum.org/archive/2015/slides/45B-Charles%20Janac.pdf, at slide 14. As a further illustration, the Arteris NoC includes pipelining for distance spanning when traveling "~6mm" has a propagation delay of "~400ps/mm", requiring at least "2400ps to span the Distance"; thus requiring "at least 3 pipeline stages and 4 clock cycles to meet timing."

U.S. Patent No. 8,072,893 (Dielissen & Rijpkema)
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	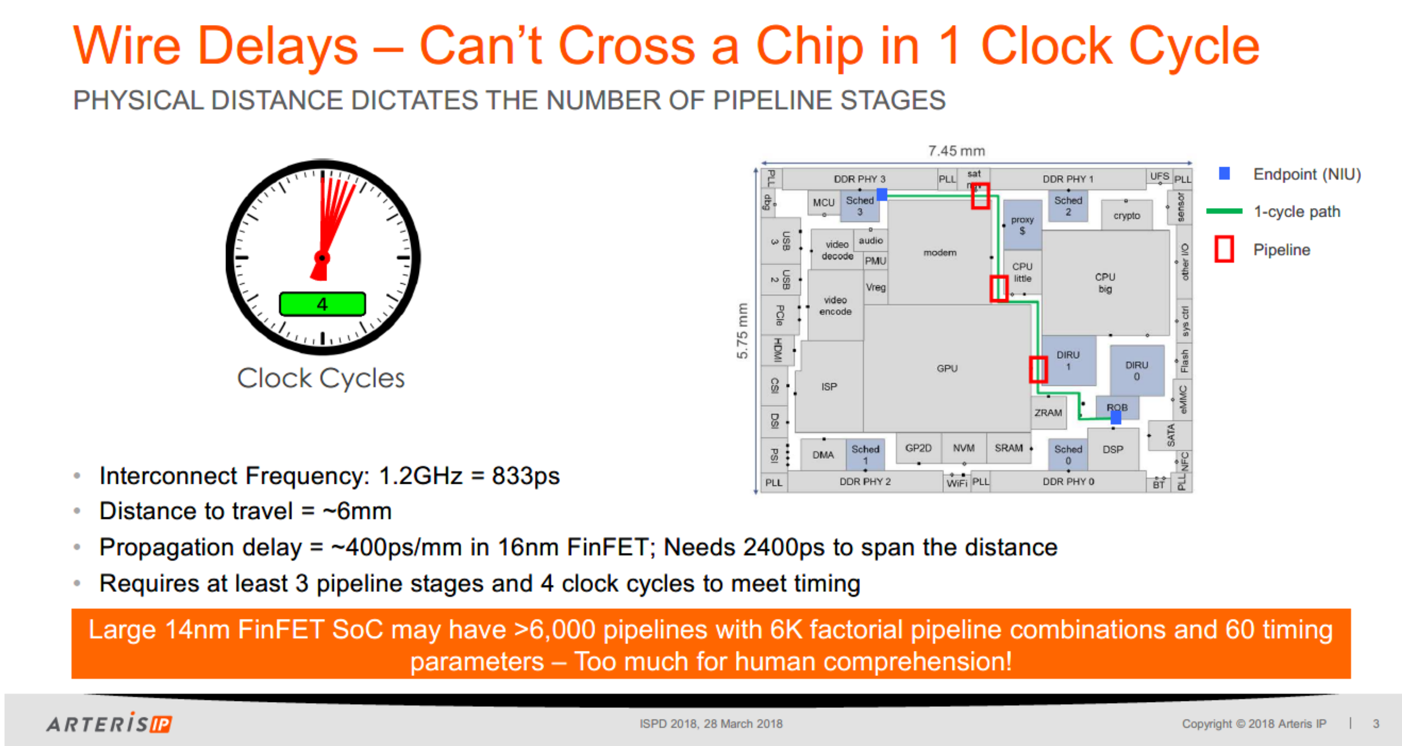 *See* Physical Interconnect Aware Network Optimizer, http://www.ispd.cc/slides/2018/s7_2.pdf, at slide 3.

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